



캐비넷저장

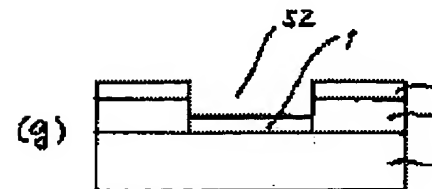
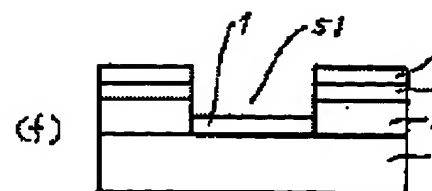
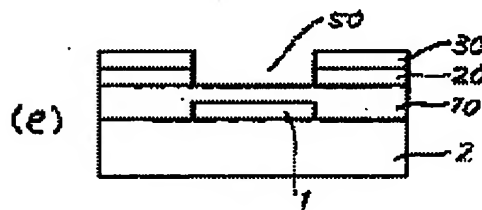
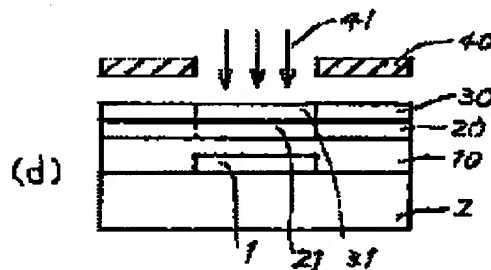
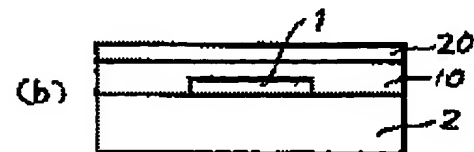
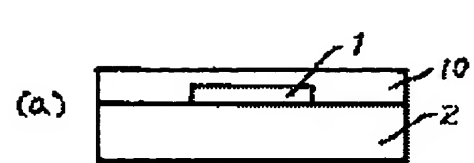
캐비넷보기



## (54) SEMICONDUCTOR INTEGRATED CIRCUIT AND MANUFACTURING METHOD THEREFOR

- (19) 국가 (Country) : JP (Japan)
- (11) 공개번호 (Publication Number) : 2001-094056 (2001.04.06) ▶ 日本語/한글(JP)  
▶ 현재진행상태보기
- (13) 문헌종류 (Kind of Document) : A (Unexamined Publication)
- (72) 발명자 (Inventor) : YOKOO KIMITAKA, MONJUJI HIROAKI
- (71) 출원인 (Applicant) : VICTOR CO OF JAPAN LTD
- (57) 요약 (Abstract) :  
 PROBLEM TO BE SOLVED: To provide a semiconductor integrated circuit that can be manufactured with a simple process and less manufacturing costs, so that a solution used in the process can be subjected easily to waste liquid treatment.  
  
 SOLUTION: In this semiconductor integrated circuit with a semiconductor integrated circuit, where a semiconductor element is formed and a protective film formed on the semiconductor integrated circuit, the protective film is made of an inorganic insulation film and an organic insulation resin with positive photosensitive property.  
  
 COPYRIGHT: (C)2001,JPO
- (21) 출원번호 (Application Number) : 1999-270115 (1999.09.24)
- (51) 국제특허분류 (IPC) : H01L-027/04 ; H01L-021/822 ; H01L-021/02 ; H01L-021/312
- FI :  
 H01L-021/02  
 H01L-021/312      N  
 H01L-027/04      A
- 테마코드 : 5F038; 5F058
- F텀 :  
 5F038: EZ03 EZ11 EZ20  
 5F058: AA10 AD02 AD04 AD08 AD10 AD11 AF04 AH01 AH03
- (30) 우선권번호 (Priority Number) : -
- 본 특허를 우선권으로 한 특허 : -
- 대표도면 : -

AL



INPADOC 패밀리 (Family 1) :

↳ 패밀리/법적상태 일괄보기

Country	Pub. No.	Kind	Pub. Date	Title
JP	2001-094056	A	2001.04.06	반도체 집적 회로 및 그 제조 방법
<input checked="" type="checkbox"/> 선택된 패밀리특허 캐비넷 저장				Basic

특허포대신청

Copyright©1998-2003 WIPS Co.,Ltd. All rights reserved.  
Tel:02-362-1288 : Fax:02-362-1289 : E-mail:wips@wips.co.kr